Series TF333-250

High Frequency Inverter grade Capsule Thyristor Type TF333-250

Low switching losses
Low reverse recovery charge
Distributed amplified gate for high di/dt

Maximum mean on-state current				I_{TAV}		**250 A**		
Maximum repetitive peak off-state				U_{DRM}		**1200 ÷ 2200 V**		
and reverse voltage				U_{RRM}				
Turn-off time				**tq**		**25; 32; 40 µs**		
U_{DRM}, U_{RRM}, V	1200	1300	1400	1500	1600	1800	2000	2200
Voltage code	12	13	14	15	16	18	20	22
Tvj, °C	- 60 ÷ 125							

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	TF333-250	Conditions
I_{TAV}	Mean on-state current	A	250 445	Tc=90 °C, Tc=55 °C, 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	392	Tc=90 °C
I_{TSM}	Surge on-state current	kA	6,3 7,0	Tvj=125°C Tvj=25°C tp=10 ms U_R=0
I^2t	Limiting load integral	kA²s	198 245	Tvj=125°C Tvj=25°C
U_{DRM}, U_{RRM}	Repetitive peak off-state and reverse voltage	V	1200÷2200	Tj мin≤Tvj≤Tjм 180° half-sine wave, 50 Hz Gate open
U_{DSM}, U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	1300÷2300	Tj мin≤Tvj≤Tjм 180° half-sine wave tp=10 ms, Single pulse Gate open
(di_T/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	1000 500	Tvj=125°C ; U_D=0,67 U_{DRM}, Gate pulse : 10V,5 Ω, 1µs rise time, 10 µs
U_{RGM}	Peak reverse gate voltage	V	5	Tj мin≤Tvj≤TjМ
Tstg	Storage temperature	°C	-60÷80	
Tvj	Junction temperature	°C	-60÷125	

CHARACTERISTICS

U_{TM}	Peak on-state voltage	V	2,8	Tvj=25°C, I_{TM}=3,14 I_{TAV}
$U_{T(TO)}$	Threshold voltage	V	1,6	Tvj=125°C
R_T	On-state slope resistance	mΩ	1,7	1,57 I_{TAV}< I_T <4,71 I_{TAV}
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	50 50	Tvj=125°C, $U_D = U_{DRM}$ $U_R= U_{RRM}$

CHARACTERISTICS

Symbols and parameters		Units	TF333-250	Conditions	
I_L	Latching current	A	5	Tvj=25°C,UD=12V Gate pulse : 10V, 5Ω, 1 μs rise time, 10μs	
I_H	Holding current	A	0,5	Tvj=25°C,UD=12V, Gate open	
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C	UD=12V
I_{GT}	Gate trigger direct current	A	0,3 0,85	Tvj=25°C, Tvj=-60°C	
U_{GD}	Gate non-trigger direct voltage	V	0,25	Tvj=125°C, UD = 0,67 UDRM	
I_{GD}	Gate non-trigger direct current	мA	10	Direct gate current	
t_{gd}	Delay time	μs	1,6	Tvj=25°C,UD=500V ITM = 250 A	
t_{gt}	Turn-on time	μs	2,5	Gate pulse : 10V, 5Ω, 1 μs rise time, 10μs	
t_q	Turn-off time	μs	25÷40 32÷50	Tvj=125°C, ITM =250 A diR/dt =10 A/μs, UR=100V UD = 0,67 UDRM duD/dt=50 V/μs duD/dt=200 V/μs	
Q_{rr}	Recovered charge	μC	350	Tvj=125°C, ITM =250 A diR/dt =50 A/μs, UR=100V	
t_{rr}	Reverse recovery time	μs	5,6		
I_{rrM}	Peak reverse recovery current	A	125		
$(du_D/dt)crit$	Critical rate of rise of off-state voltage	V/μs	500 1000	Tvj=125°C, UD = 0,67 UDRM Gate open	
R_{thjc}	Thermal resistance junction to case	°C/W	0,045	Direct current, double side cooled	

ORDERING

	TF	333	250	20	7	5	3	
	1	2	3	4	5	6	7	

1. Fast thyristor with interdigitated gate structure.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (20=2000V).
5. Critical rate of rise of off-state voltage (6 ≥ 500 V/μs, 7 ≥1000 V/μs).
6. Group of turn-off time (duD/dt=50 V/μs, 3 ≤ 40 μs, 4 ≤ 32 μs, 5 ≤ 25 μs).
7. Group of turn-on time (3 ≤ 2,5 μs).
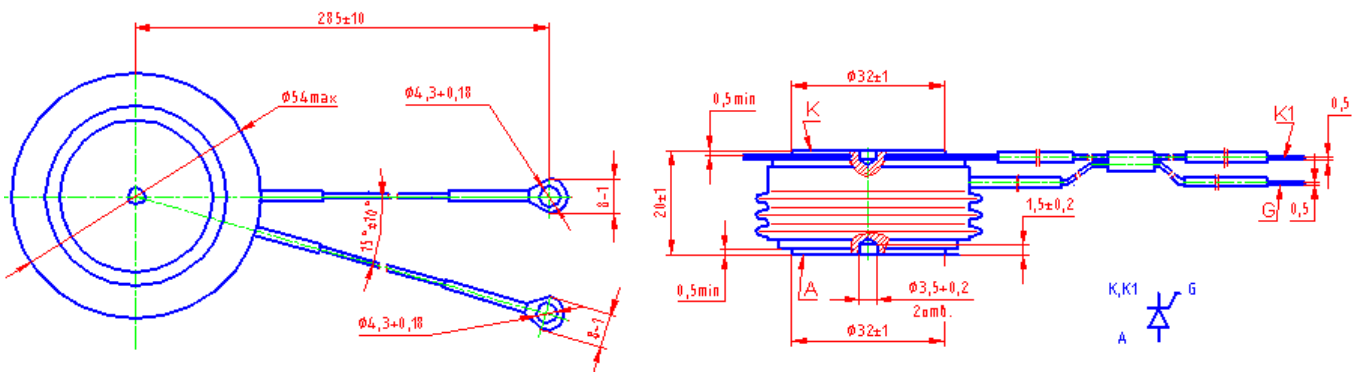
Mounting force : 9÷14 kN
Weight : 190 grams